Improving the Characteristics of Integrated EMI Filters by Embedded Conductive Layers

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***Abstract*—Discrete electromagnetic interference (EMI) filters have been used for power electronics converters to attenuate switching noise and meet EMI standards for many years. Because of the unavoidable structural parasitic parameters of the discrete filter components, such as equivalent parallel capacitance (EPC) of inductors and equivalent series inductance (ESL) of capacitors, the effective frequency range of the discrete filter is normally limited. Aiming at improving high frequency performance and reducing size and profile, the integrated EMI filter structure has been proposed based on advanced integration and packaging technologies [1], [2]. Some improvements have been made but further progress is limited by EPCs of the filter inductors, which is restricted by dimension, size and physical structure. In this paper, a new structural winding capacitance cancellation method for inductors is proposed. Other than trying to reduce EPCs, a conductive ground layer is embedded in the planar inductor windings and the structural capacitance between the inductor winding and this embedded layer is utilized to cancel the parasitic winding capacitance. In order to obtain the best cancellation effect, the structural winding capacitance model of the planar spiral winding structure is given and the equivalent circuit is derived. The design methodology of the layout and area of the embedded ground layer is presented. Applying this method, an improved integrated EMI filter is designed and constructed. The experimental results show that the embedded conductive layer can effectively cancel the parasitic winding capacitance, hence ideal inductor characteristics can be obtained. With the help of this embedded conductive layer, the improved EMI filter has much smaller volume and profile and much better characteristics over a wide frequency range, compared to the former integrated EMI filter and the discrete EMI filter.**

***Index Terms*—Electromagnetic interference (EMI), equivalent parallel capacitance (EPC), equivalent series inductance (ESL).**

I. Introduction

POWER electronics has been continuously driven by improved power semiconductor devices, improved circuit topologies, increased switching frequency and advanced packaging and integration technologies in the last decades. As the switching frequency increases, the problem of electromagnetic interference (EMI) is increased. The requirement of reducing size, weight and cost drives the circuits to be smaller and smaller. More circuits have been crowded into less space, which also increases the probability of interference. The conventional discrete EMI filter has been used for switch mode power supplies to attenuate switching noise and meet the EMI standard for many years. However, because of the unavoidable structural parasitic parameters of the discrete filter components, such as equivalent parallel capacitance (EPC) of inductors and equivalent series inductance (ESL) of capacitors, shown in Figs. 1 and 2, the effective frequency range of the discrete filter is normally limited. The manufacturing and assembling of the wire wound, toroidal shape inductor is labor intensive, results in increased cost and reduced reliability. By using advanced integration and packaging technologies, integrated EMI filters have been proposed to improve high frequency performance and reduce size and profile [1], [2]. All the filter components can be integrated into one module, constructed by using standard semiconductor processing, printed circuit board (PCB) and packaging techniques, which are all low labor content manufacturing procedures. EPCs of the integrated EMI filter was greatly reduced by using a staggered and interleaved winding structure, resulting in improved common mode (CM) filter performance. This is briefly covered in Section III. However, further reducing EPCs is restricted by size, profile, structural and material limitations. Also, the staggered and interleaved winding structure complicates the manufacturing processes and increases the total winding thickness, compromising the advantages of the integrated EMI filters. In this paper, instead of trying to reduce the structural winding capacitance, which is very difficult for the planar structure, a new winding capacitance cancellation method is proposed. The basic principle is presented and a simplified equivalent circuit is derived. To apply this winding capacitance canceling method to integrated EMI filters, a conductive layer is embedded between the planar inductor winding layers. The structural capacitance between the embedded layer and the inductor windings is utilized to cancel the structural winding capacitance. In order to obtain the best canceling effect, the layout and area of the embedded layer must be optimally designed. The necessary structural winding capacitance model of the planar winding structure is derived. Based on this model, the optimal embedded layer area is calculated. Applying this method, an integrated EMI filter with this embedded conductive layer is constructed. The experimental results show that by using this embedded conductive layer, nearly ideal filter inductor characteristics can be obtained. The new integrated EMI filter has reduced profile and volume and much better high frequency characteristics, as compared to the discrete EMI filter and the former integrated EMI filters [1], [2].

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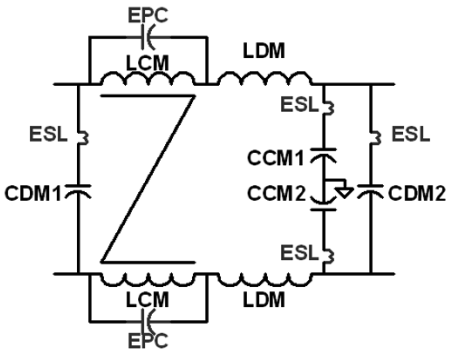


Fig. 1. Schematic of EMI filter.

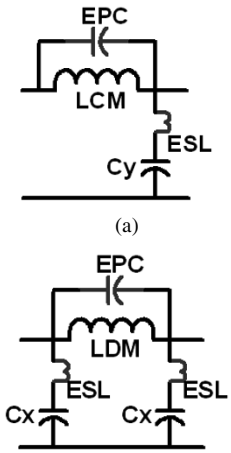


Fig. 2. (a) Equivalent circuit of CM filter. (b) Equivalent circuit of DM filter.

II. Structural Winding Capacitance of Filter Inductors

The schematic of a typical EMI filter is shown in Fig. 1. Its common mode (CM) and differential mode (DM) equivalent circuits are shown in Fig. 2(a) and (b). As can be seen, the CM and DM filters are all basic LC low pass filters. The filter inductor is normally a wire wound toroidal inductor. It can be well characterized in a wide frequency range by the equivalent circuit seen in Fig. 3(a). The resistance R_s in the equivalent circuit represents the losses of the coil and magnetic core. Sometimes a parallel resistance R_p is used, shown in Fig. 3(b), to represent the winding loss and core loss. Parasitic effects at higher frequencies, resulting from the stray capacitances between turns, cannot be neglected. Although the turn to turn and layer to layer capacitance is distributed, a parallel connected concentrated capacitor provides a suitable approximation. The impedance of the choke coil according to the equivalent circuit shown in Fig. 3(a) is

$$Z_L = \frac{R + j\omega L}{1 - \omega^2 LC + j\omega RC}. \tag{1}$$

Its impedance versus frequency is shown in Fig. 4. Because of the parasitic winding capacitance, the attenuation of a LC low pass filter reduces at high frequencies, as illustrated in a typical transfer function of a LC low pass filter, shown in Fig. 5. For a CM filter, where the filter capacitance [C_y in Fig. 2(a)] is limited by the safety requirement of the leakage current, the inductance of the coil is normally in the range of a few mH, which makes

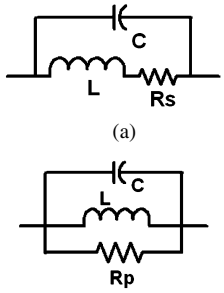


Fig. 3. (a)Equivalent circuit 1 of a choke. (b) Equivalent circuit 2 of a choke.

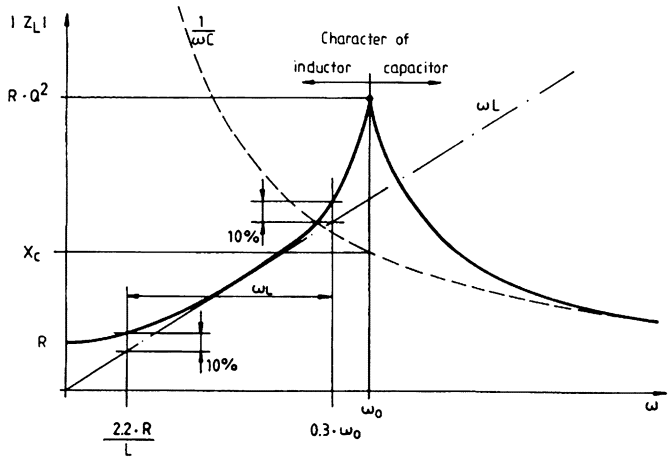


Fig. 4. Impedance versus frequency of a choke [8].

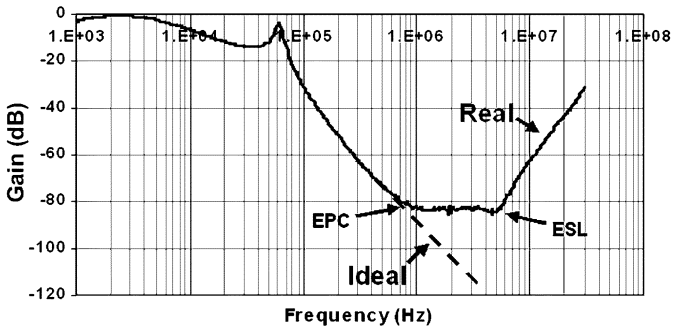


Fig. 5. Typical transfer gain of LP filter.

the structural winding capacitance of the coil the most critical parasitic parameter because a very small parasitic capacitance can bring the effective inductor frequency down to a few hundred kHz. To improve the high frequency characteristics of inductors, the structural winding capacitance has to be minimized. However, because of the structural, electromagnetic and material limitations, the parasitic capacitance can only be reduced to a certain value, typically 10–20 pF for a conventional winding structure, and there is no way to completely eliminate it. This is even worse for the planar spiral winding inductors because the increased winding surface area and increased number of winding layers will greatly increase the structural ("parasitic") winding capacitance. To shrink the size, lower the profile and improve the high frequency characteristics of discrete EMI filters, the integration of EMI filters were presented in [1], [2] and will be briefly discussed in the next section.

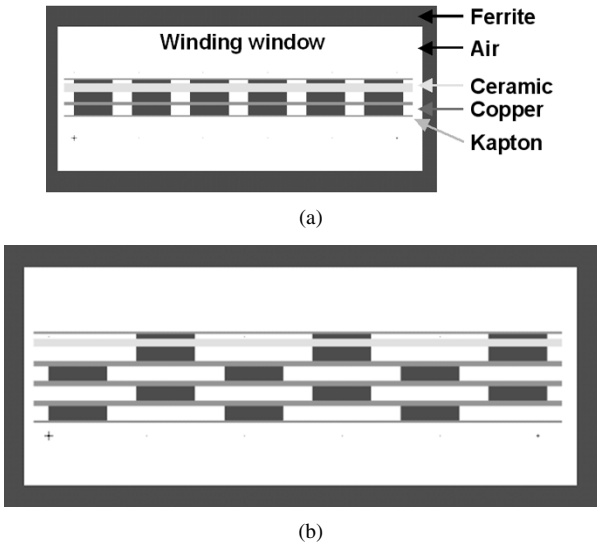


Fig. 6. (a) Original Structure. (b) Staggered winding structure.

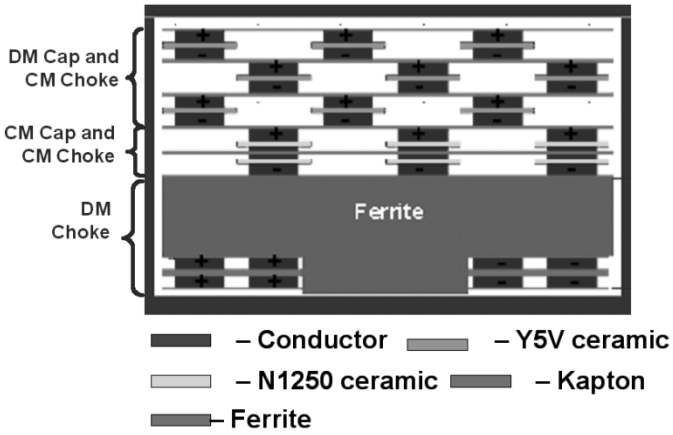


Fig. 7. Cross-sectional view of the half winding window of an integrated EMI filter structure.

III. Review of Previous Integrated EMI Filters

The formerly developed planar spiral winding integrated LC technology is applied to integrate the EMI filter capacitors and inductance, by using the low-pass filter configuration of the planar Integrated L-C structure [1], [2]. However, since functions of the high frequency power passive components and the EMI filter are different in SMPS circuits, their requirements are accordingly different. Power passive components, such as HF transformers, inductors and capacitors, need to store and transfer energy at switching frequency. On the contrary, although EMI filter also consists of passive components, it needs to attenuate energy at switching frequency and its harmonics. Hence, the major requirement for the integrated EMI filter is improving high frequency characteristics, which can be realized by reducing the equivalent parallel capacitance (EPC) of the inductors and the equivalent series inductance (ESL) of the equivalent capacitors of the integrated module to increase HF attenuation, and increasing high frequency conductor losses to increase HF damping [4]–[7].

The technologies to reduce ESL and increase high frequency conductor losses of integrated EMI filters have been presented in [1], [2], the detailed description and analysis can be referred to [9]. To reduce EPC, a staggered winding structure is used, as shown in Fig. 6. By utilizing the staggered windings, the EPC of a constructed prototype is reduced from originally around 100 pF to around 10 pF. Interleaving technique is required for the integrated two-winding planar CM choke to reduce EPC caused by close magnetic coupling. However, the leakage inductance is also greatly reduced because of interleaving. Additional windings and magnetic cores have to be inserted to implement the DM inductor. By applying these technologies, an integrated EMI filter structure was presented in [2]. Its front cross-section view of half winding window is shown in Fig. 7 to illustrate the integration structure. The detailed description and equivalent circuit can be referred to [1], [2], [9].

The staggered and interleaved winding structure discussed in [1], [2] can effectively reduce the parasitic winding capacitance, but at the price of greatly increased winding complexity and increased thickness. Since it is impossible to totally eliminate and difficult to reduce the parasitic winding capacitance, shifting and canceling it will be an alternative and better way to solve the problem.

IV. Canceling of Structural Winding Capacitance

In order to cancel or shift the detrimental structural winding capacitance, additional circuitry or components has to be added. The circuit shown in Fig. 8(a) is proposed. In this circuit, the inductor L_f in a low pass filter is tapped, represented by two perfectly coupled inductors (each has 1/4 of the total inductance) in series, and the center point is connected to ground through a capacitor C_g. The distributed structural winding capacitance is represented by a lumped capacitor C_e. To simplify the analysis, the parallel resistance R_p shown in Fig. 3(b) is neglected temporarily. Applying the decoupled T equivalent circuit of the coupled inductors [see Fig. 8(b)] and the Y/∇ transformation [see Fig. 8(c)], the L_1, L_2, C_e, and C_g sub network can be simplified to the π equivalent circuit shown in Fig. 8(d), where Y_1, Y_2, and Y_{12} are

$$Y_1 = Y_2 = \frac{1}{2} j\omega C_g \tag{2}$$

$$Y_{12} = \frac{1 + \frac{1}{4}\omega^2 LC_g - \omega^2 LC_e}{j\omega L}. \tag{3}$$

It is shown that when $C_g = 4C_e, Y_{12} = 1/j\omega L$, is the admittance of a perfect inductor, which means the parasitic winding capacitance is completely canceled. The detailed analysis considering the losses, the coupling coefficient, the parametric study, sensitivity study, circuit simulation and experimental verification are outside the confines of this paper.

As must be mentioned that the added grounding capacitance C_g not only can be implemented by an external lumped capacitor, it can also be implemented by utilizing the parasitic capacitance between windings and ground. To control and obtain the desired C_g, a conductive ground layer can be embedded between winding layers. With the insertion of this ground plane (which doesn't have to cover all the winding surface), the electric field energy stored in the stray field in the winding window is redistributed, which can be approximately divided into two parts: the energy stored in the field (W_{E1}) between the winding layers and the inserted ground layer [represented by lumped capacitance C_g in Fig. 8(a)] and the energy stored in the field (W_{E2}) between winding layers where the windings are not covered by the inserted ground layer [represented by C_e in Fig. 8(a)], shown in Fig. 10(d). As the ground layer

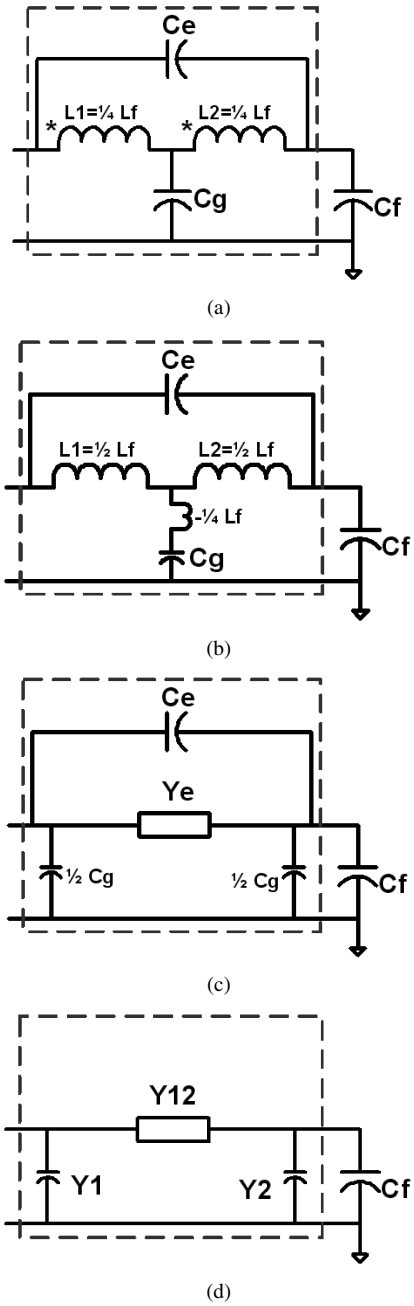


Fig. 8. (a) Schematic of inductor w/parasitic capacitance canceling. (b) Decoupled equivalent circuit. (c) Y/Δ transformation results. (d) π equivalent circuit.

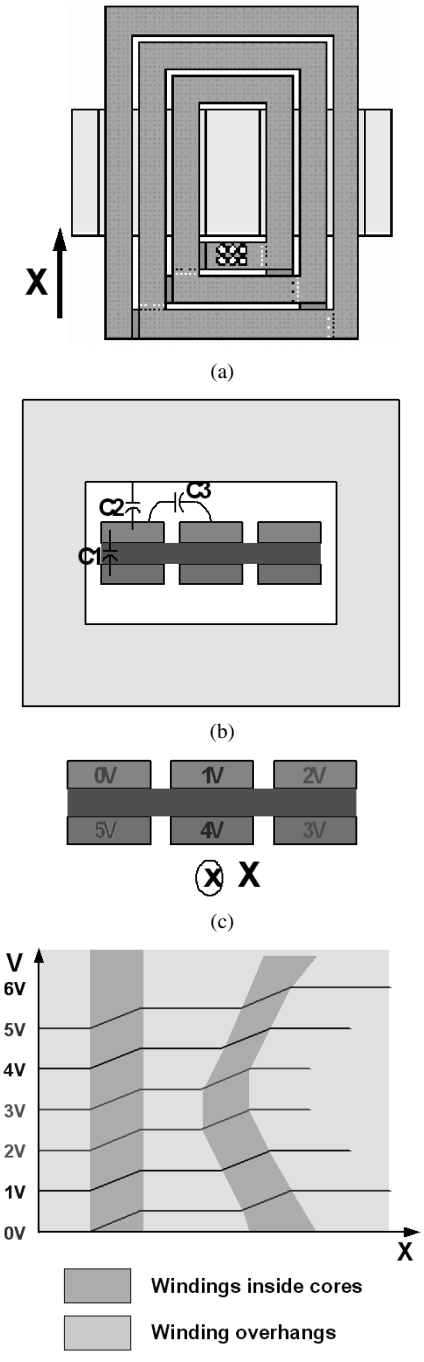


Fig. 9. (a) Top view of cross section of a planar spiral winding. (b) Front view of cross section of half winding window. (c) Voltage distribution of cross section—front view. (d) Voltage distribution along winding length.

area increases, more energy is stored in W_{E1}, hence C_g is increased. At the same time, since the un-shielded winding area is decreased, less energy is stored in W_{E2}, resulting in smaller C_e. It implies that there is an optimal ground layer area where $C_g = 4C_e$. To obtain this optimal point, the structural winding capacitance model of planar spiral winding structure is derived, since implementation of this solution is much more feasible in a planar winding structure.

V. Structural Winding Capacitance Model of Planar Spiral Winding Structure

The top and front cross-section view of a typical planar spiral winding structure is shown in Fig. 9(a) and (b). To simplify the derivation procedure, a two layer, three turns per layer structure is used as an example, but the results can be applied to other multi-layer, multi-turn structures as well. In Fig. 9(b), C_1 represents the distributed capacitance between layers, C_2 represents the distributed capacitance between windings and core, C_3 represents distributed capacitance between turns. In most cases, C_2 can be neglected, because normally the distance between windings and core is much larger than the insulation thickness between winding layers. The turn to turn capacitance C_3 can be calculated by using the Schwarz-Christoffel transformation [3]. If the permittivity of the substrates (insulation) material is not

high (FR4, Kapton...), C_3 is normally much smaller than C_1, hence can also be neglected. The layer to layer capacitance C_1 is calculated based on the following assumptions.

1) Since for most practical multilayer planar inductors with magnetic cores, the winding layers are magnetically coupled very closely, which means the leakage inductance between layers is much smaller than the magnetizing inductance. Hence the leakage inductance can be neglected.
2) Since in the conducted EMI frequency rang (150 kHz–30 MHz), the impedance of the equivalent winding resistance is much smaller than that of the inductance, hence it can be neglected.
3) Based on the previous two assumptions, it is shown that the winding voltage distribution is determined by the inductance per turn. For most practical planar inductors with spiral windings and regular magnetic core shape, the inductance per turn is constant. Therefore, the voltage is linearly distributed along the winding length [noted as X in Fig. 9(a), (c), and (d)].
4) Since for most practical planar spiral winding inductors with planar E cores, the overhang conductor is not surrounded by magnetic material, hence, its inductance is much smaller than the inductance of the conductors in the core window. Therefore, the voltage drop on overhang conductors can be neglected.

Based on the above assumptions, the voltage profile of the example inductor is shown in Fig. 9(c)–(d). Fig. 9(c) shows the front cut-view of the winding layers. The different number on each conductor indicates the sequence of winding turns. The number also represents the potential of the each turn at the beginning point, assuming 1 V/turn. Fig. 9(d) shows the voltage profile of each turn along the winding length direction (X direction). Each turn is represented by a curve with its potential number corresponded to Fig. 9(c). The length of each turn is different and needs to be calculated separately since the lateral dimension of planar spiral windings has to be considered. It is shown in Fig. 9(d) that even though the voltage is changing along winding length, the voltage difference between every two vertically adjacent conductors is a constant. For an example, the voltage between conductor one and four is always 3 V along the X direction.

Knowing the voltage distribution, the electrical field energy stored between two vertically adjacent conductors (the ith and $(2m-1-i)$th conductor) can be calculated, given by

$$W_{\mathrm{Em}} = \frac{1}{2} \cdot C_0 \cdot l_i \cdot (2i-1)^2 \tag{4}$$

where l_i is the winding length of the ith turn, m is the number of turns per layer, C_0 is the capacitance per unit length of each turn, given by

$$C_0 = \frac{\varepsilon_0 \varepsilon_r w}{d} \tag{5}$$

where w is the conductor width, d is the insulation thickness, and ε_r is the relative permittivity of the insulation material.

The total stored electric field energy of all the layers is

$$W_E = \left(\frac{n}{m} - 1\right) \cdot \sum_{i=1}^{m} \frac{1}{2} \cdot C_0 \cdot l_i \cdot (2i-1)^2 \tag{6}$$

TABLE I
PARAMETERS OF A PLANAR INDUCTOR PROTOTYPE

Core size	*Conductor width (mm)*	*Insulation thickness (mm)*	ε_r	*Calculated Ce (pF)*	*Extracted Ce (pF)*
Planar E38 + PLT 38	0.8	0.05	3.6	123	118

where n is the total number of turns. The lumped equivalent structural capacitance is given by

$$C_e = \frac{2W_E}{n^2}. \tag{7}$$

To verify this model, a two layer, six turns per layer planar inductor prototype was constructed and measured. Its structural winding capacitance is experimentally extracted from the curve fitting results of the impedance measurement using HP4194A impedance/gain-phase analyzer. The physical parameters and the calculated and extracted winding capacitance values are listed in Table I. It is evident that the calculated value matches the experimentally extracted result well.

VI. DESIGN OF THE EMBEDDED CONDUCTIVE LAYER FOR INTEGRATED EMI FILTER

The cross section view of a planar inductor with embedded conductive layer is shown in Fig. 10(a). An example winding layout and embedded layer layout is shown in Fig. 10(b). From its physical structure, the equivalent circuit can be derived, shown in Fig. 11(a). In Fig. 11(a), the lumped capacitance C_1–C_4 represent the distributed capacitance between winding layers and the embedded ground plane, $C_1 = C_2 = C_3 = C_4 = 1/2C$, where C is the total structural capacitance between one of the winding layers and the embedded ground plane. R_3 and L_3 represent the impedance of the ground plane. In the frequency range of interest of the conducted EMI standard (150 kHz–30 MHz), the impedance of the ground plane can normally be neglected. This results in a simplified equivalent circuit shown in Fig. 11(b). Following the same procedure as given in Section IV, it can be derived that when $C = 4C_e$, the structural winding capacitance C_e can be completely canceled. Assuming the width of the embedded ground layer is fixed and is equal to the winding window width, the length X (along the winding length direction, same as X-direction given in Fig. 9) of the embedded layer can be chosen as the design variable [shown in Fig. 11(c)]. C and C_e as a function of X are given by

$$C_e = \frac{\left(\frac{n}{m} - 1\right) \cdot \sum_{i=1}^{m} \frac{\varepsilon_0 \varepsilon_r W_w}{h_1} \cdot (l_i - X) \cdot (2i-1)^2}{n^2} \tag{8}$$

where W_w is the width of the winding conductor, h_1 is the thickness of the insulation material between two winding layers, ε_r is the relative permittivity of the insulation material

$$C = \frac{m \varepsilon_0 \varepsilon_r W_w X}{h_2} \tag{9}$$

where h_2 is the thickness of the insulation material between winding layer and the embedded ground plane.

For the parameters used by the designed integrated EMI filter prototype, the relationship of C_e and (1/4)C as a function of X is plotted in Fig. 12. The point where the two lines cross

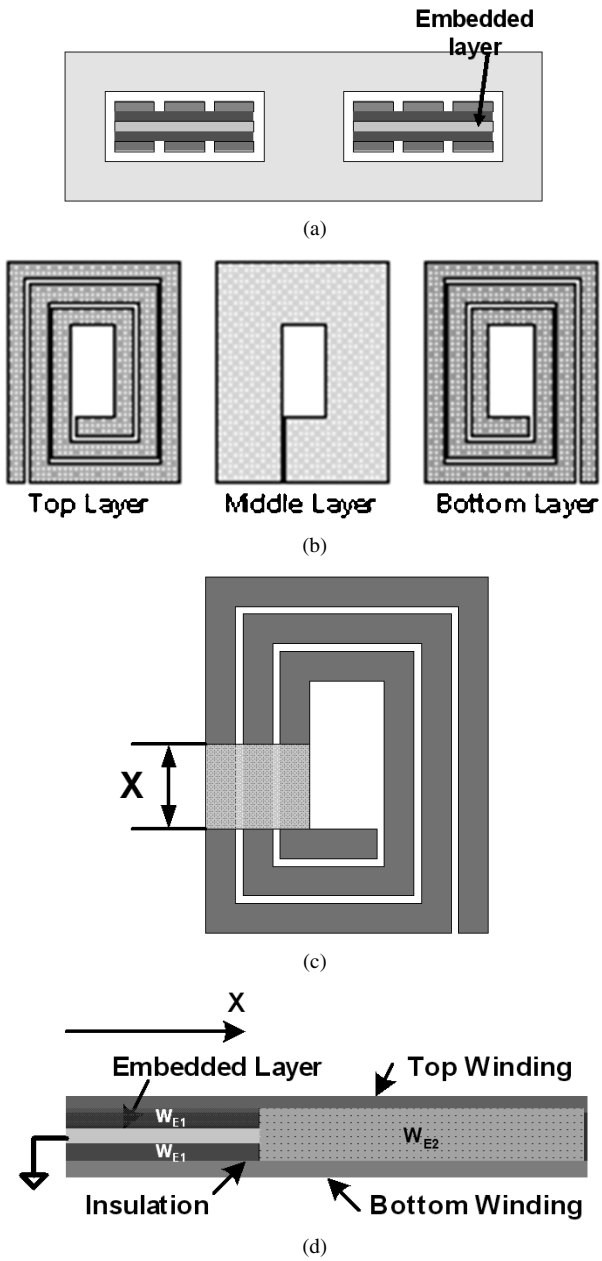


Fig. 10. (a) Planar winding w/embedded layer. (b) An example of winding and embedded layer layout. (c) Definition of design variable "X." (d) Side cross-section view of windings with embedded layer.

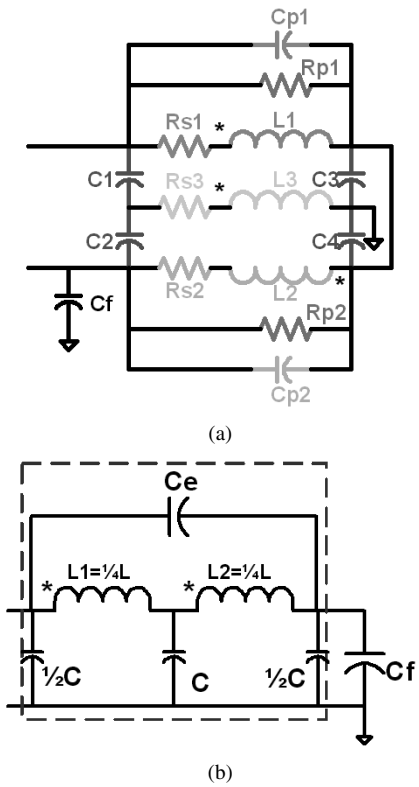


Fig. 11. (a) Equivalent circuit of planar inductor w/embedded layer. (b) Simplified equivalent circuit.

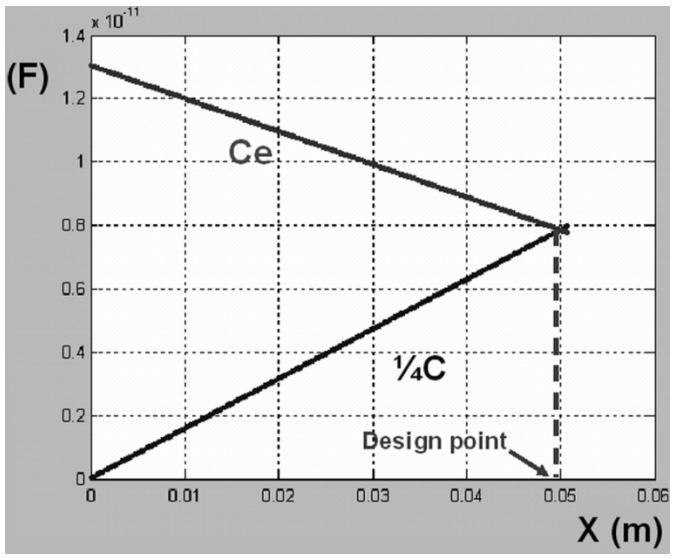


Fig. 12. C_e and C versus X.

indicates the optimal design point and the correspondent $X =$ 49 mm is chosen as the designed embedded ground plane length. For the designed integrated EMI filter prototype, the width of the embedded layer is equal to the winding window width of a planar E38 core ($\approx$ 10 mm) and its thickness is approximately 70 μm (2.8 mils).

To verify this design, an L–C low-pass filter with a planar filter inductor and a discrete ceramic capacitor is constructed, as shown in Fig. 13. The planar inductor has the same magnetic core structure and winding structure as those of the inductors of the integrated EMI filter. The parameters are given in Table II. The small signal transfer functions of this filter with and without the embedded conductive layer are measured by using an HP 4194A impedance/gain phase analyzer. The measurement setup is referred to the next section. The results are shown in Fig. 14. It is evident that with the designed embedded layer, the structural winding capacitance of the inductor is almost completely cancelled.

VII. Experimental Results

Applying the proposed method, an improved integrated EMI filter with embedded conductive layer is designed and constructed. The detailed integrated EMI filter design procedure can be found in [1]. The DM choke inductance is implemented by utilizing the leakage inductance of the CM choke windings.

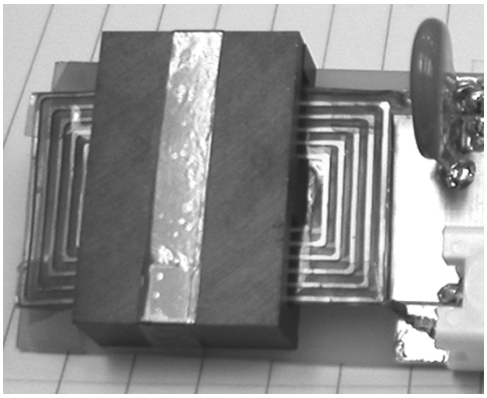
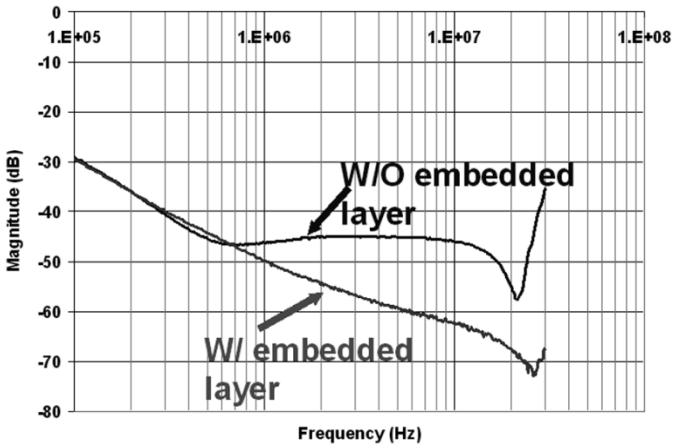
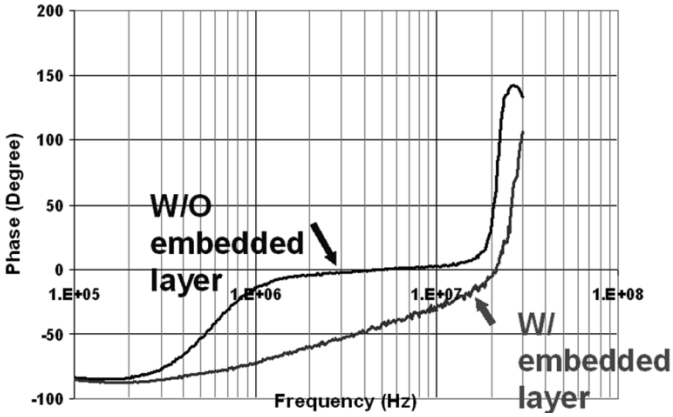


Fig. 13. Low-pass filter with planar inductor.



(a)



(b)

Fig. 14. (a) Measured transfer gain of the low-pass filter prototype: gain. (b) Measured transfer gain of the low-pass filter prototype: phase.

A leakage layer made of ferrite polymer composite (FPC) material is inserted between the two CM choke windings to increase the leakage inductance. The design procedure of the leakage layer can be referred to [1]. The front cross section view of the half winding window of the improved integrated EMI filter with embedded layer is shown in Fig. 15. As must be pointed out that although the leakage layer is inserted, the magnetic coupling coefficient of the layers of each winding is not changed much. This is because firstly, the leakage layer is made of the low permeability FPC material (μr =9) and the windings

TABLE II
PARAMETERS OF A LOW-PASS FILTER

Parameters	*Value*
Inductor core size	Planar E38 + PLT 38
Core material	3E5
Number of turns	12
Number of turns per layer	6
Inductance (mH)	4.5
Capacitance (nF)	3.3

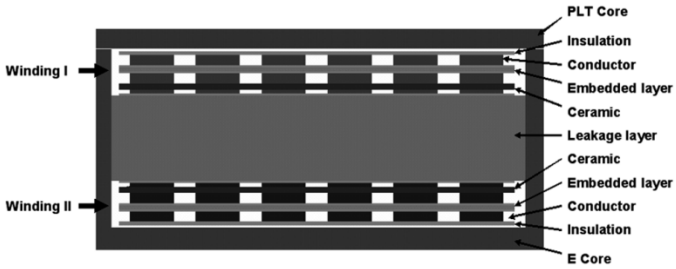
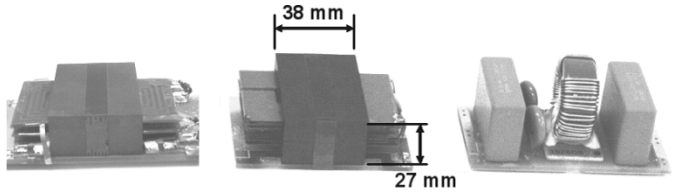


Fig. 15. Cross section view of half winding window of improved integrated EMI filter.



(a) (b) (c)

Fig. 16. Constructed prototypes: (a) improved integrated EMI filter, (b) previous integrated EMI filter, and (c) discrete EMI filter.

are surrounded by high permeability ferrite 3E5 (μr = 10 000). Secondly, as shown in Fig. 15, the leakage layer is placed between the two CM choke windings (not inside any single winding). Therefore, the coupling coefficient between layers of the winding itself is nearly unchanged. Hence the assumption in V can still hold and the derived model is valid. The constructed prototypes are shown in Fig. 16. The component parameters and size comparisons with the previous integrated EMI filter [1], [2] and the discrete EMI filter are listed in Table III. The baseline discrete EMI filter is an input line filter of a commercial 1-kW power factor correction (PFC) converter product. The parameters are extracted from the small signal impedance and transfer-gain measurement results, according to the analysis in [10]–[14]. In both integrated EMI filters, capacitance is integrated by applying the low-pass filter configuration of the planar spiral winding integrated LC structure [1], [2]. The transfer gains of the improved integrated EMI filter, previous integrated EMI filter and discrete EMI filter are measured by using a HP 4194A impedance/Gain-phase analyzer. To reduce the influence of other parasitic parameters, all the prototypes are mounted on a test board with minimized lead length, minimized input and output loop area. The input and output ports are leaded out by using 3 GHz BNC connectors. The signal

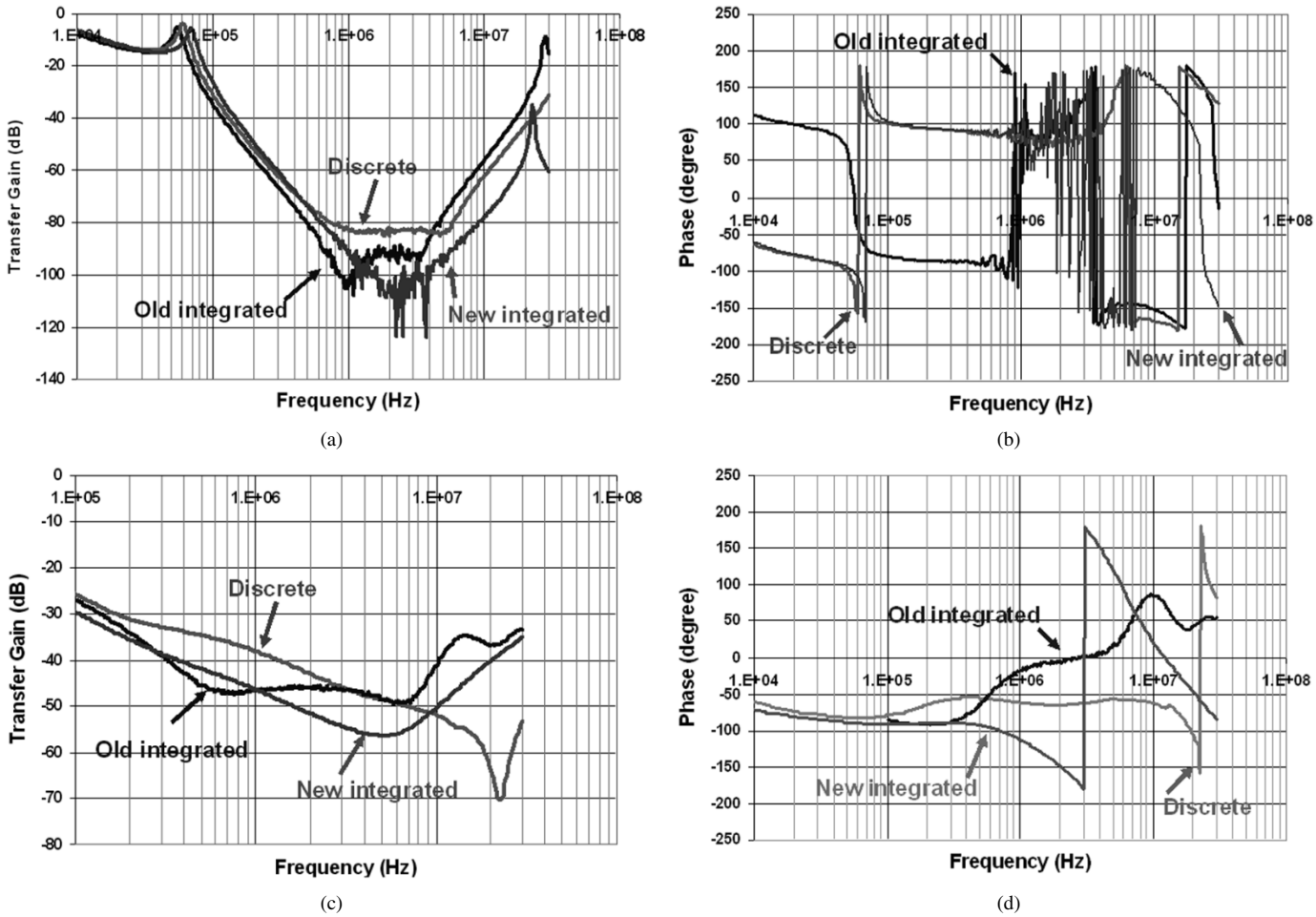


Fig. 17. (a) DM transfer functions: gain. (b) DM transfer functions: phase. (c) CM transfer functions: gain. (d) CM transfer functions: phase.

TABLE III
PARAMETER AND SIZE COMPARISONS OF EMI FILTERS

Parameters	*Improved integrated*	*Previous integrated*	*Discrete*
LCM (mH)	4.5	3.1	3.3
LDM (uH)	21	21	16.7
CCM (nF)	6.6	6	6.6
CDM (μF)	0.7	0.7	0.68
EPC (μF)	Canceled	17	12
ESL (nH)	Less than 10	30	70
No. of components	1	1	5
Profile (cm)	1.2	1.6	2.6
Volume (cm^3)	20	27.4	39.8

source impedance and the load impedance are set to real 50-Ω standard value (set internally in the impedance analyzer). The measurement results are shown in Fig. 17. It is evident that the improved integrated EMI filter has the smallest size and profile, but much better CM and DM characteristics over a wider frequency range than those of the previous integrated EMI filter and the discrete EMI filter. The structural winding capacitance is effectively canceled by using the embedded conductive ground layer, which is a very simple solution without increasing the complexity of the winding structure. Therefore, the CM characteristics of the new integrated EMI filter are much better than that of the old one.

VIII. CONCLUSION

In this paper, the problem of improving the characteristics of integrated EMI filter is addressed. Instead of trying to reduce the parasitic winding capacitance, which is construction limited, a new method is proposed for structural winding capacitance cancellation. For a planar winding structure, which is the magnetic structure used in the integrated EMI filters, a conductive ground layer can be inserted between winding layers to achieve the parasitic winding capacitance cancellation. The structural capacitance between the windings and the embedded layer is utilized. In order to obtain the best cancellation results, the layout and area of the embedded ground layer has to be optimally designed. The structural winding capacitance model of the planar winding structure and the design methodology of the embedded ground layer are proposed and verified by experimental results. Based on the proposed method, an improved integrated EMI filter is designed and constructed. The experimental results show that using this method, much improved inductor characteristics can be obtained. With the help of this parasitic capacitance canceling method, the improved integrated EMI filter has much smaller size and profile, but much better CM and DM characteristics over a wider frequency range than those of the former integrated EMI filter and the discrete EMI filter.

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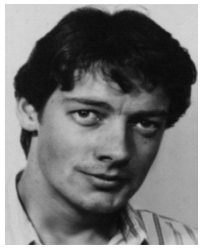

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